WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a first insulating layer, the first insulating layer comprising a first dielectric material and a second dielectric material formed over the first dielectric material, the second dielectric material comprising a different material than the first dielectric material;

a plurality of first conductive regions formed in the first dielectric material, the first conductive regions comprising a first pattern; and

a plurality of second conductive regions formed in the second dielectric material, the second conductive regions comprising a second pattern, the second pattern being different from the first pattern.

2. The semiconductor device according to Claim 1, wherein the first dielectric material comprises an organic material, and wherein the second dielectric material comprises an inorganic material.

3. The semiconductor device according to Claim 1, wherein the first dielectric material comprises an inorganic material, and wherein the second dielectric material comprises an organic material.

4. The semiconductor device according to Claim 1, wherein the plurality of first conductive regions comprise vias, and wherein the plurality of second conductive regions comprise conductive lines.

5. The semiconductor device according to Claim 4, wherein the vias have sidewalls, wherein the sidewalls of the vias are substantially vertical.

6. The semiconductor device according to Claim 1, wherein the second dielectric material comprises SiLK^{TM} or porous-SiLK^{TM}, and the first dielectric material comprises undoped silicate glass (USG), fluorinated silicon glass (FSG), fluorinated tetraethoxysilate (FTEOS), SiCOH, or porous-SiCOH.

7. The semiconductor device according to Claim 1, wherein the first dielectric material comprises a material that is etchable selective to the second dielectric material.

8. The semiconductor device according to Claim 1, further comprising a hard mask disposed over the second dielectric material.

9. The semiconductor device according to Claim 8, wherein the hard mask comprises two or more layers.

10. The semiconductor device according to Claim 9, wherein the hard mask comprises a layer of SiC_x, SiC_xN_y, SiC_xH_y, $SiC_xN_yH_z$, or SiCOH disposed over the second dielectric material, a layer of Si_xN_y or SiO_2 disposed over the layer of SiC_x, SiC_xN_y, SiC_xH_y, $SiC_xN_yH_z$, or SiCOH, and a layer of refractory metal nitride disposed over the layer of Si_xN_y or SiO_2.

11. The semiconductor device according to Claim 10, wherein the layer of SiC_x, SiC_xN_y, SiC_xH_y, $SiC_xN_yH_z$, or SiCOH comprises a first layer of SiC_x and a second layer of N-SiC_x disposed over the first layer of SiC_x.

12. The semiconductor device according to Claim 1, wherein the first insulating layer is disposed over a plurality of conductive lines in a second insulating layer.

13. The semiconductor device according to Claim 12, wherein the conductive lines comprise copper, wherein the first dielectric layer comprises a material having a coefficient of thermal expansion (CTE) close to the CTE of the conductive lines.

14. The semiconductor device according to Claim 13, further comprising a cap layer disposed over the second insulating layer.

15. The semiconductor device according to Claim 15, wherein the cap layer comprises Si_xN_y, N-SiC_x, SiC_x, SiC_xH_y, $SiCOH_x$, $SiC_xN_yH_z$, SiN_xH_y, or combinations thereof.

16. The semiconductor device according to Claim 1, further comprising an adhesion film disposed over a top surface of the cap layer.

17. A semiconductor device, comprising:

a workpiece;

a first insulating layer disposed over the workpiece;

a plurality of first conductive lines formed in the first insulating layer;

a second insulating layer formed over the first conductive lines and the first insulating layer, the second insulating layer comprising a first dielectric material and a second dielectric material formed over the first dielectric material, the second dielectric material comprising a different material than the first dielectric material;

a plurality of vias formed in the first dielectric material; and

a plurality of second conductive lines formed in the second dielectric material.

18. The semiconductor device according to Claim 17, wherein the first dielectric material comprises an organic material, and wherein the second dielectric material comprises an inorganic material.

19. The semiconductor device according to Claim 17, wherein the first dielectric material comprises an inorganic material, and wherein the second dielectric material comprises an organic material.

20. The semiconductor device according to Claim 17, wherein the vias have sidewalls, wherein the sidewalls of the vias are substantially vertical.

21. The semiconductor device according to Claim 17, wherein the second dielectric material comprises a material that is etchable selective to the first dielectric material.

22. The semiconductor device according to Claim 17, wherein the first dielectric material comprises a material that is etchable selective to the second dielectric material.

23. The semiconductor device according to Claim 17, further comprising a hard mask disposed over the second dielectric material.

24. The semiconductor device according to Claim 23, wherein the hard mask comprises two or more layers.

25. The semiconductor device according to Claim 24, wherein the hard mask comprises a layer of SiC_x, SiC_xN_y, SiC_xH_y, $SiC_xN_yH_z$, or SiCOH disposed over the second dielectric material, a layer of Si_xN_y or SiO_2 disposed over the layer of SiC_x, SiC_xN_y, SiC_xH_y, $SiC_xN_yH_z$, or SiCOH and a layer of refractory metal nitride disposed over the layer of Si_xN_y or SiO_2.

26. The semiconductor device according to Claim 25, wherein the layer of SiC_x, SiC_xN_y, SiC_xH_y, $SiC_xN_yH_z$, or SiCOH comprises a first layer of SiC_x and a second layer of N-SiC_x disposed over the first layer of SiC_x.

27. The semiconductor device according to Claim 17, wherein the first conductive lines comprise copper, wherein the first dielectric layer comprises a material having a coefficient of thermal expansion (CTE) close to the CTE of the first conductive lines.

28. The semiconductor device according to Claim 17, further comprising a cap layer disposed over the first insulating layer.

29. The semiconductor device according to Claim 28, wherein the cap layer comprises Si_xN_y, N-SiC_x, SiC_x, SiC_xH_y, $SiCOH_x$, $SiC_xN_yH_z$, SiN_xH_y, or combinations thereof.

30. The semiconductor device according to Claim 28, further comprising an adhesion film disposed over a top surface of the cap layer.

31. The semiconductor device according to Claim 17, further comprising an adhesion film disposed over a top surface of the first dielectric layer.

32. The semiconductor device according to Claim 17, wherein the second dielectric material comprises SiLK^{TM} or porous-SiLK^{TM}, and the first dielectric material comprises undoped silicate glass (USG), fluorinated silicon glass (FSG), fluorinated tetraethoxysilate (FTEOS), SiCOH, or porous-SiCOH.